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Claims

[c1] 1. A thin-film resistor comprising a conductor layer formed on a surface, said conductor layer comprising end portions tapered at an angle less than about 90 degrees with respect to the surface to provide contact regions for coupling to said thin-film resistor.

[c2] 2.The thin-film resistor of claim 1, wherein said angle is between about 20 degrees to about 70 degrees.

[c3] 3.The thin-film resistor of claim 2, wherein said angle is between about 40 degrees to about 50 degrees.

[c4] 4.The thin-film resistor of claim 1, wherein said conductor layer comprises tantalum nitride.

[c5] 5.The thin-film resistor of claim 4, wherein said conductor layer has a thickness of from about 45 nm to about 55 nm.

[c6] 6.The thin-film resistor of claim 1 further comprising a dielectric layer formed on said conductor layer.

[c7] 7.The thin-film resistor of claim 6, wherein said dielectric layer comprises silicon nitride.

[c8] 8.The thin-film resistor of claim 7, wherein said dielectric layer has a thickness of from about 65 nm to about 75 nm.

[c9] 9.The thin-film resistor of claim 1 further comprising contacts abutting said contact regions to provide for electrical coupling to said thin-film resistor.

[c10] 10.A method of fabricating a thin-film resistor on a substrate, comprising the steps of:
providing a substrate comprising a dielectric layer having an upper
surface;
forming a conductor layer on the upper surface;
patterning a masking layer on said dielectric layer; and
removing exposed portions of said conductor layer to provide end portions
of said conductor layer that are tapered at an angle less than about 90 degrees with respect to the upper surface.

[c11] 11.The method of claim 10, wherein said angle is between about 20 degrees to about 70 degrees.

[c12] 12.The method of claim 11, wherein said angle is between about 40 degrees to about 50 degrees.

[c13] 13.The method of claim 10, wherein said step of forming said conductor layer comprises depositing a layer of tan-

talum nitride.

[c14] 14.The method of claim 10 further comprising forming a dielectric layer on said conductor layer prior to said step of patterning.

[c15] 15.The method of claim 10, wherein said step of patterning comprises exposing and developing a photoresist layer.

[c16] 16.The method of claim 10, wherein said step of removing comprises a reactive ion etch comprising Cl2 and BCl3 gases.

[c17] 17.The method of claim 10 further comprising the step of forming contacts coupled to said end portions.

[c18] 18.A semiconductor structure comprising:
a substrate comprising a plurality of interconnects formed on an upper
surface of an inter-metal dielectric layer; and
a thin-film resistor comprising a conductor layer formed on the upper
surface of said inter-metal dielectric layer and adjacent to a first of said plurality of interconnects, said conductor layer comprising end portions tapered at an angle between about 20 degrees to about 70 degrees with respect to the upper surface to provide contact regions for

coupling to said thin-film resistor.

[c19] 19.The structure of claim 18, wherein said conductor layer comprises tantalum nitride.

[c20] 20.The structure of claim 18, wherein said plurality of interconnects comprise aluminum or aluminum alloys.